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Analysis and Design of Finfet Based Variable Gain Amplifier

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ABSTRACT
Comparison of analog figures-of-merit of FinFETs and MOSFETs reveals an interesting tradeoff in the analog/RF design space. It is found that FinFETs possess the following key advantages over MOSFETs: reduced power dissipation, and better voltage gain without degradation of noise or linearity. This makes them attractive for low-frequency RF applications around 5 GHz, where the performance-power tradeoff is important. On the other hand, in high-frequency applications, planar bulk MOSFETs is seen to hold the advantage over FinFETs due to their higher peak transconductance. However, this comes at a cost of a reduced voltage gain of bulk MOSFETs.
Keywords: Analog, FinFET, MOSFET, radio-frequency (RF), silicon-on-insulator (SOI) technology.

I. INTRODUCTION

As the semiconductor industry continues towards scaling transistors into the 45 nm technology node and beyond, it is confronted with serious challenges like diminishing gate control over the channel, which manifests itself in the form of increased short-channel effects (SCE) and leakage currents [1]. To counter these effects, new materials is introduced for improved performance, either into the gate stack, the channel, or the source/drain extensions regions. However, even with the introduction of these new materials, leakage will continue to be a serious problem. Hence, alternate device architectures are being explored which possess inherently better robustness to SCE like multiple-gate FETs, also known as FinFETs or gate wrap-around FETs, are emerging as strong candidates [2]–[4]. In a FinFET, the gate wraps around a thin slice of (preferably undoped) silicon, also known as a "fin", and current flows along the top and side surfaces of the fin. This wrap-around nature of the gate enhances the gate control over the channel, thus reducing the SCE and leakage currents. A drawing of the FinFET showing its important geometrical parameters is shown in Fig. 1. Scaling improves digital performance in accordance with Moore's law; analog performance is affected in many ways. For the classical planar bulk MOSFET, the analog performance does benefit from improvements in transconductance as a result of scaling. However, this is accompanied by a degraded output conductance and voltage gain. FinFETs, on the other hand, have been shown to have potential for analog applications [5], [6]. Lightly doped or undoped fin body increases carrier mobility. Short channel length enables velocity overshoot, which increases mobility. Low Vth decreases the vertical electric field, which increases carrier mobility. Tunneling effects such as Gate to channel tunneling, Band to band tunneling at PN junction is present in FinFET. A raised source/drain structure can be used to reduce the parasitic resistance. However, the overlap capacitance is increased. Parasitic resistance is the main adverse factor which prevents finfets' application, which leads to lower speed and high noise. Main advantages of FinFETS are having excellent control of short channel effects in submicron regime and making transistors still scalable. Due to this reason, the small- length transistor can have a larger intrinsic gain compared to the bulk counterpart. Much Lower off-state current compared to bulk counterpart. Promising matching behavior. Applications of FinFET are Low power design in digital circuit, such as RAM, because of its low off-state current. Also used as a Power amplifier or other application in analog area this requires good linearity [1].

This paper explores the analog-performance tradeoffs of variable gain amplifier using planar bulk MOSFET and FinFET architectures from the device performance point of view, and the resulting consequences for RF circuit design. The paper is organized into a section on current steered variable gain amplifier, followed by a result discussion, and conclusions.

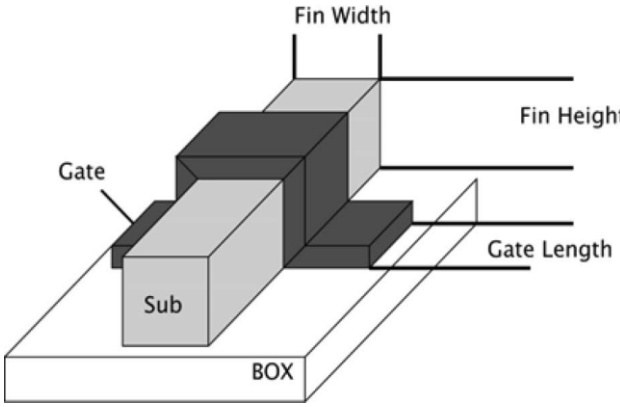

Fig 1: Drawing of the FinFET device indicating the main geometrical parameters, namely, gate length, fin width, and fin height [1].

II. VARIABLE GAIN AMPLIFIER

Variable gain amplifiers (VGAs) have a wide range of applications in electronic systems, especially in those requiring an automatic gain control loop. In communication systems, they play an indispensable role in receivers by controlling the incoming signals power level and normalizing the average amplitude of the signal to a reference value. This helps in optimizing system capabilities and reducing the complexity of circuits. Automatic gain control circuit configurations require three key components that are employed in all or most architectures: a variable gain amplifier, a peak signal detector and a gain control voltage generation circuit. The AGC core cell is the variable gain amplifier. This cell determines the main properties of the complete AGC, such as the frequency response, gain range and distortion, and this is the reason for its importance. It is a signal-conditioning amplifier with settable gain: the VGA adjusts -amplifying or attenuating- the incoming signal to the desired optimal level according to a gain function, G(VC), which depends on a control signal *VC* provided by the AGC loop. The VGA directly affects the main AGC specifications, such as bandwidth, noise and harmonic distortion. Ideally, to obtain the best overall performance, the VGA should neither limit the frequency operation nor the linearity of the system. As a consequence, in the design of the AGC, meeting the VGA requirements is usually the most challenging task. When the gain is varied continuously, the amplifier takes the generic name "VGA". In contrast, if the gain is varied digitally the amplifier is called "Programmable Gain Amplifier" or "PGA". A Schematic of the V-band VGA topology based on the cascode structure is shown in Fig.2 An auxiliary nMOS transistor is used in the cascode structure which overcome the linearity issue at the low gain state and enlarge the gain control range. This auxiliary nMOS transistor compensates the third-order intermodulation distortion current component generated by the common-gate stage of the cascode structure. Thus, larger gain control range and higher linearity are achieved simultaneously.

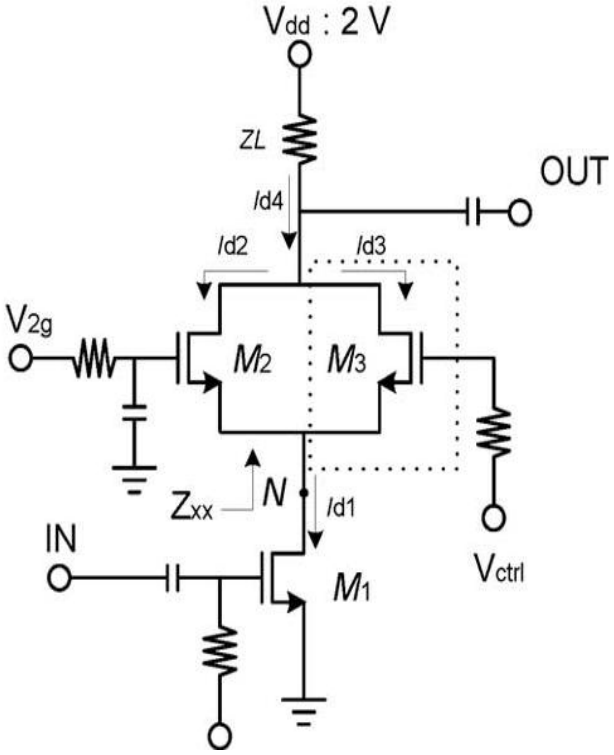

Fig 2: Schematic of the VGA topology [7]

III. RESULT AND DISCUSSION

The supply voltage applied is 2 V and Vctrl varies from 0 to 2 V.V2g is set carefully to 1.5 V because it affects the current steering mechanism. Bias voltage to gate of M1 is set as 0.55v, and load resistance is set to 200Ω. Fig. 3 illustrates the current distribution in MOSFET M2 and M3 when it is scaled by 32nm with different size of M3. M3 is sized to 3µm, 6µm and 23µm, and Fig.4 shows simulated power gain with various Vctrl at 60 GHz.Fig.5 shows current distribution in FinFET X2 and X3 when length is 32nm with different size of X3. X3 is sized to 72nm, 144nm and 576nm, and Fig.6 shows simulated power gain with various Vctrl at 60 GHz. Table I shows the comparison of performance of variable gain amplifier using MOSFET when replaced with FinFET. Power dissipation of variable gain amplifier reduces and voltage gain improves by using FinFET. The current steering point reduces by using finFET.

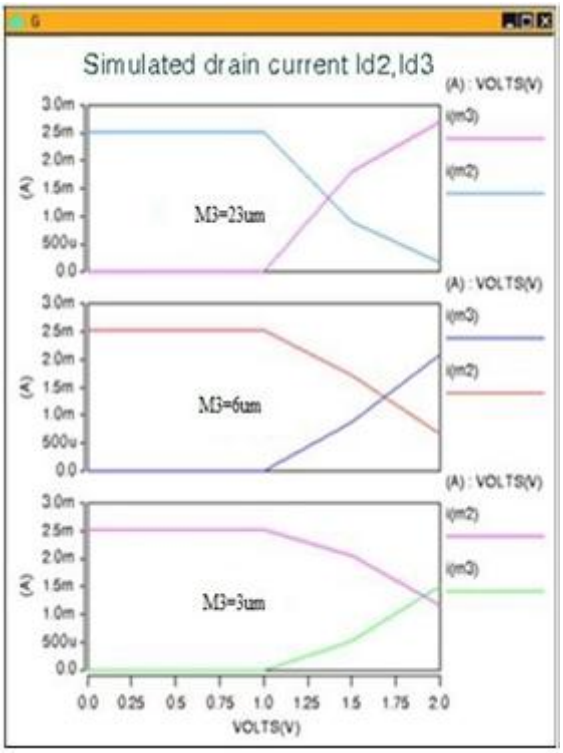

Fig 3: Simulated drain current Id2 and Id3 of the MOSFET at low frequencies (L=32nm).

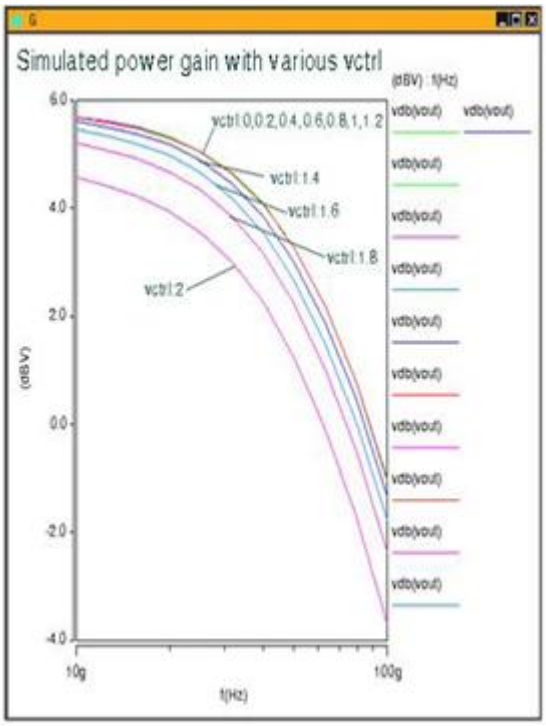

Fig 4: Simulated power gain with various Vctrl at 60 GHz (m1 = 6µm, m2 = 12µm, and m3 = 6µm).

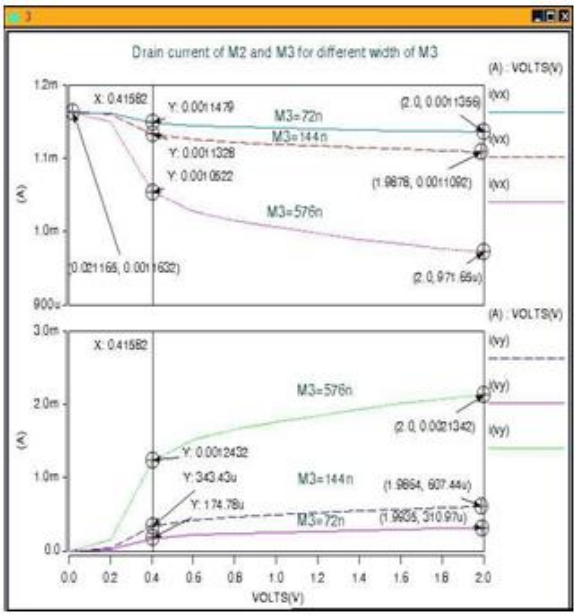

Fig 5: Simulated drain current Id2 and Id3 of the FINFET at low frequencies (L=32nm).

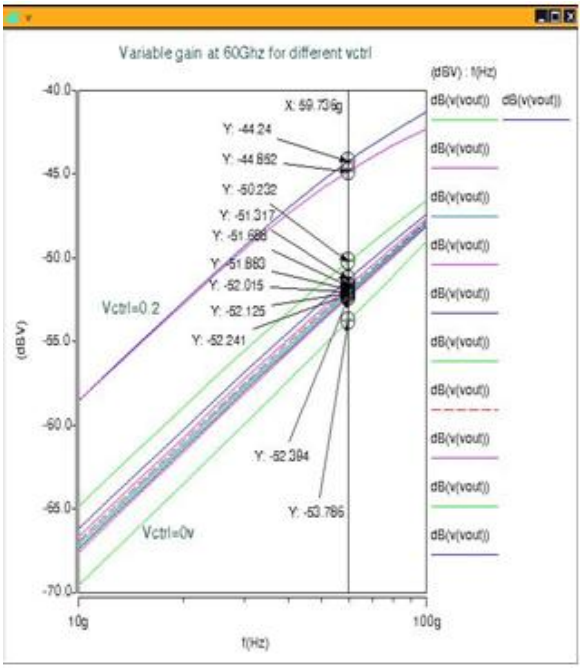

Fig 6: Simulated power gain of FINFET with various Vctrl at 60 GHz (X1 = 144nm, X2 = 288nm, and X3 = 144nm).

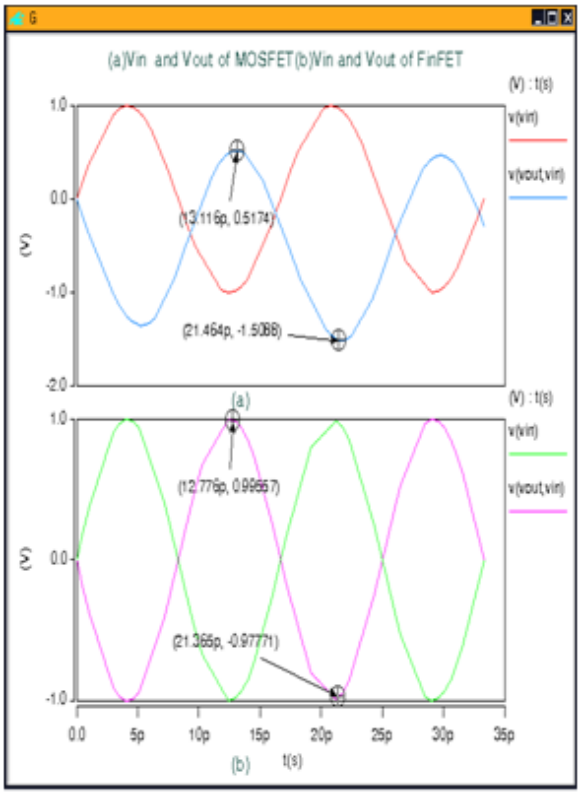

Fig 7 :(a) Vin and Vout of MOSFET (b) Vin and Vout of FinFET

Table 1. Comparison of variable gain amplifier performance characteristics

Parameter	MOSFET	FINFET
Maximum current in high gain state	2.5mA	1.1632mA
Minimum current in low gain state	250µA, 500µA, 1mA	1.1356mA, 1.11092mA, 0.97166mA
Current steering point	1.25v,1.7v,1.95v for different M3	0.2v
Maximum current in low gain state	2.5mA,2mA,1.5mA For different M3	2.1342mA,0.6021mA, 0.310mA for differentM3
Supply voltage	2V	2V
Power dissipation	1.50mw	590.1865uw
Variable gain range	Gain is constant for Vctrl (0-1.2v) & varies from (1.4-2v)	Gain varies when Vctrl varies from (0-2v)

IV. CONCLUSION

We have demonstrated that FinFET technology, where a silicon-on-insulator (SOI) technology fin has several key advantages over planar bulk MOSFET technology. Threshold voltage is lower due to a reduced bulk (depletion) capacitance. Owing to the narrow fin widths and wrap-around nature of the gates, the fins are fully depleted, which results in a much reduced modulation of the depletion region by the drain voltage. This result in an output conductance, which is lower compared to MOSFETs, and translates into a much higher voltage gain. All this makes FinFETs attractive for low frequency (5 GHz) RF applications biased around a gate voltage overdrive of 0.2 V, where the performance-power tradeoff is important. In variable gain amplifier using FinFET gain varies for Vctrl 0v-2v, but FinFETs suffer from a high series resistance, which degrades the drive current and transconductance. The impact of this series resistance is amplified at high gate voltage overdrives, and as a result, for high-frequency applications, bulk MOSFETs are seen to hold the advantage over FinFETs due to their lower series resistance and higher peak transconductance. By using FinFET power dissipation also reduces for the same supply voltage.

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